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U. S. PATENT DOCUMENTS

EXAMINER INITIAL	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLA SS	SUBCLASS	FILING DATE
JC	*2002 0 039051	April 4, 2002	Ota Yoshiyuki et al.			
JC	*6,351,191	February 26, 2002	Nair Rajendran et al.			
				-		

Copy of reference is not enclosed because reference is cited and described in Search Report (copy of reference provided by the International Searching Authority).

FOREIGN PATENT DOCUMENTS

						TRANSLATION	
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Yes	No
				-			1

OTHER DOCUMENTS

EXAMINER INITIAL	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
JC	Kaenel V Von et al: "A VOLTAGE REDUCTION TECHNIQUE FOR BATTERY-OPERATED SYSTEMS" IEEE Journal of Solid-State Circuits, IEEE Inc. New York, US, Bd. 25, Nr. 5, 1 October 1990 (1990-10-01), Seiten 1136-1140, XP000162795 ISSN: 0018-9200*
JC	Zhang Z-X et al: "A 360 MHZ 3V CMOS PLL WITH IV PEAK-TO-PEAK POWER SUPPLY NOICE TOLERANCE" IEEE International Solid State Circuits Conference, IEEE Inc. New York, US Bd. 39, 1 February 1996 (1996-02-01), Seiten 134-135,431, XP000685566 ISSN: 0193-6530*

Copy of reference is not enclosed because reference is cited and described in Search Report (copy of reference provided by the International Searching Authority).

EXAMINER	/Joseph Chang/	DATE CONSIDERED	02/07/2007

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